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Buckled Thin-Film Transistors and Circuits on Soft Elastomers for Stretchable Electronics

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ABSTRACT. Although recent progress in the field of flexible electronics has allowed the realization of biocompatible and conformable electronics, systematic approaches which combine high bendability (< 3 mm bending radius), high stretchability (> 3-4 %) and low complexity in the fabrication process are still missing. Here, we show a technique to induce randomly-oriented

and customized wrinkles on the surface of a biocompatible elastomeric substrate, where Thin-Film Transistors (TFTs) and circuits (inverter and logic NAND gates) based on Amorphous-IGZO are fabricated. By tuning the wavelength and the amplitude of the wrinkles, the devices are fully operational while bent to 13 μm bending radii as well as while stretched up to 5%, keeping unchanged electrical properties. Moreover, a flexible rectifier is also realized, showing no degradation in the performances while flat or wrapped on an artificial human wrist. As proof of concept, transparent TFTs are also fabricated, presenting comparable electrical performances to the non-transparent ones. The extension of the buckling approach from our TFTs to circuits demonstrates the scalability of the process, prospecting applications in wireless stretchable electronics to be worn or implanted.

KEYWORDS: buckles, stretchable electronics, indium-gallium-zinc-oxide, thin-film transistors, circuits, transparent electronics, rectifier.

INTRODUCTION. The demand for flexible, lightweight and high-performance electronics is continuously growing. The broad range of applications in the field of flexible electronics includes smart textiles,[1,2] curvy imaging devices,[3-5] and biomedical integrated systems [6-8] for medical implants. Within this scenario, the research trend is mainly focused towards three directions: increased bendability, where devices show functionality down to bending radii of tens of micrometers;[9, 10] low weight, where ultra-thin membranes are employed as substrate, for conformable devices capable of laying onto any 3D surface;[11] biocompatibility, which allows applications, such as the surgical implantation of any electronics for health monitoring.[12, 13] Although these studies have shown impressive results in the last years, the development of

systematic techniques and/or approaches which can be implemented for stretchable circuits is even more challenging. In recent works, transfer processes have been employed to place ultra-thin membranes (thickness ~ 1 μm) on highly stretchable supports [14, 15] such as, locally reinforced composited. In this way, the applied strain is mechanically decoupled from the electronic devices, with the drawback of an additional transfer step with raise the fabrication complexity. With this method, photovoltaic cells, as well as Thin-Film Transistors (TFTs) have shown excellent functionality and high flexibility (stretchability > 20%). Another approach consists in the fabrication of electronic devices directly on an engineered flexible substrate, containing structured rigid platforms.[16] Finally, the realization of "wavy" electronics devices, such as a-Si TFTs,[17] polymer-based LEDs (PLEDs) [3] and matrix tactile sensors,[18] is generally obtained by releasing the initial strain applied on the flexible substrate.[19]

Here, we demonstrate a technique to control the formation of superficial and randomly-oriented wrinkles with variable amplitude and wavelength on the surface of a Polydimethylsiloxane (PDMS) substrate. In particular, the thermal strain, induced in the flexible membrane when cured on a rigid support, as well as the duration of an oxygen treatment is tuned. By modifying the geometrical size of the wrinkles (wavelength and amplitude), flexible TFTs and circuits (inverter and logic NAND gate) are realized directly fabricated on the elastomeric membrane. Once the device fabrication is complete, the buckling of the soft elastomer is allowed by the selective dissolution in water of a sacrificial layer. In this way, the wrinkled electronics, based on amorphous Indium-Gallium-Zinc-Oxide (a-IGZO), can be bent down to 13 μm, as well as stretched up to 5%. Furthermore, a stretchable and biocompatible wrinkled diode bridge rectifier circuit based on IGZO (as n-type semiconductor) and NiO (as p-type semiconductor) is also shown. Tested in flat condition and wrapped around an artificial

human wrist, the circuits yield no degradation in the performances. Finally, wrinkled and transparent TFTs are realized as proof of concept, showing transmittance up to 71.6%. These results demonstrate a customized technology for biocompatible and flexible devices relevant for future applications, such as wireless health monitoring, sensor readouts and digital signal processing.

RESULTS AND DISCUSSIONS.

Buckling process. Different techniques have been adopted to create large-area surface wrinkles on PDMS.[20] Theoretical models [21, 22] and experiments on buckled metal lines [23-25] have been extensively studied to achieve highly stretchable conductors. The buckling can be induced by heating, solvent swelling and mechanical stress (compression or tension).[26] In our case, the mechanical properties of the flexible membrane can be tuned by two processes: surface oxidation prior the device fabrication and the substrate shrinkage caused by thermal stress. The O_2 plasma treatment is performed to modify the hydrophobic nature of the PDMS surface [27, 28] and increase the adhesion with the device layers. In this way, the elastomeric surface resembles a silica layer, with thickness proportional to the oxidation time.[29-31] This procedure results in surface wrinkles. By varying the oxidation time, a proportional increase of the wrinkle dimensions (amplitude and wavelength) is observed (see Fig. S1). On the other hand, the wrinkle formation is also due to the release of thermal stress induced in the PDMS. Differently from other temperature-driven processes, where the top surface of the soft polymer tends to expand during the deposition of a hard layer,[32] here the dominant effect is the difference of the thermal expansion coefficients between the Silicon wafer, acting as support during the fabrication, and the elastomeric substrate

(α_{Si}= 2.55 x 10^{-6} K^{-1} [33] and α_{PDMS}= 3 x 10^{-4} K^{-1}).[29] Once the latter is spin coated and cured, thermal stresses are induced in the PDMS after it has cooled down to room temperature, because the adhesion between the wafer and the elastomer, force it to remain under tensile strain during the entire device fabrication. In this way, by modifying the curing temperature (from room temperature to 180°C), the thermal intrinsic stress in the PDMS is modulated (see Fig. S1). To facilitate the release of the flexible membrane, the Silicon wafer is coated with a water soluble PVA layer, acting as sacrificial layer (see *Substrate preparation* section). Next, the fabrication of TFTs and circuits is realized using standard UV photolithographic process directly on the soft substrate, allowing resolution down to 5 μm. Both lift-off and wet etching processes are implemented for the structuring of the device stack. The semiconductor is a 15 nm-thick layer of amorphous-IGZO, while 50 nm Al_2O_3 deposited by atomic layer deposition, acts as gate dielectric. The metal contacts are formed by evaporating 35 nm thin film of Ti, for the gate, and 50 nm of Cu, for the source and drain (see *Device Fabrication* section). After the fabrication, in order to detach the elastomeric membrane from the carrier wafer, and consequently release the thermal stress, the sacrificial layer is dissolved in water, as presented in previous works [34, 35] (see Fig. S2). At this point, the flexible substrate relaxes and a temperature-dependent surface area reduction occurs, inducing the formation of a network of out-of-plane wrinkles. A schematic of the buckling process and of the TFT structure (materials and layer thicknesses) is presented in Fig. 1a. The induced strain is evaluated by measuring the length of metal segments, before and after the release process. Considering ε_x and ε_y as the strain in x- and y- direction (see Fig. S3), these values can be modulated according to the curing temperature. It should be noticed that the influence of the sacrificial layer can be ignored, since the Silicon carrier wafer has dominant

mechanical properties (Si: thickness = 200 μm, Young's modulus = 130 GPa; PVA: thickness = 100 nm, Young's modulus = 41 MPa).[35, 36]

Simulations. For the fabrication of active electronic devices using the wrinkle approach presented here, it is crucial to understand the maximum strain in the dielectric layer. Cracks, pinholes or damages in this layer, due to the buckling process, can permanently harm the device performance. For this reason, a key point is to theoretically estimate the strain induced in the Al_2O_3 and deeply understand the dominant mechanical effect, which is the strain due to the PDMS curing temperature. A model, in which PDMS has been simulated with 50 nm-thick Al_2O_3, is presented in Fig. 1b. In this case, two main assumptions are made: first, the PDMS thickness is much greater than the one used for the dielectric layer; secondly, no strain is allowed in z-direction. By simulating only the surface area reduction occuring when the flexible substrate is released from the carrier wafer, a maximum negative temperature variation $\Delta T = -150$ °C is considered. This value is meant to resemble the experimental case when the thermal stress is first induced in the elastomeric membrane (due to a maximum curing temperature of 180 °C), and then released (at room temperature, with the buckling phenomenon). Here, no assumptions for the oxygen plasma treatment are done. The analytic and Finite Element solutions provide the simulated wrinkle profile, shown in Fig. 2c. The strain tensor ε for the 50 nm-thick Al_2O_3 is evaluated, and the 2D colored map of its x-component ε_{11} is presented. Here, a continuous alternation of tensile strains ($\varepsilon > 0$), 0%-strain regions and compressive strains ($\varepsilon < 0$) is shown along the wrinkle profile (see Fig. 1b). In Fig. S4, the value of ε_{11} is shown along a single wrinkle, at two different depths: at the top surface, and at the interface with the PDMS. As

expected, the two plots alternate tensile (strain $\varepsilon > 0$) and compressive strain (strain $\varepsilon < 0$) and their values (ranging from -0.52% to 0.52%) are lower than the maximum strain ever reported for electronic circuits based on oxide semiconductors (strain $\varepsilon = 1.89\%$).[37, 38] The use of conservative parameters in the calculation of the simulated wrinkle profile (Fig. S4), to overestimate the strain in the Al_2O_3 layer, is the reason for the difference with the experimental calculation (Fig. S1).

Device buckling. The combination of both effects (surface oxidation and curing temperature) allows the wrinkling of all the layers deposited on the elastomeric substrate. A wrinkled logic NAND gate fabricated on PDMS substrate and released from the carrier wafer is shown in Fig. 1c. Its channel region is characterized by a sinusoidal-like profile with wavelength and amplitude equal to 15.28 μm and 1.3 μm, respectively (see Fig. S5). As a consequence, the flexibility of the entire device, in terms of capability to sustain mechanical strain, can be modulated according to the requirements of the application.

Bending and stretching experiments.

Bending. To prove the effectiveness of the wrinkled approach, different electronic devices are fabricated and afterwards characterized while mechanical strain is applied. For this section, all devices are fabricated on a 80 μm-thick PDMS substrate, cured at 180 °C on a 2-inch Silicon carrier wafer, and the oxidation, prior to the fabrication, is performed for 1 minute. As presented in other works, the dissolution of the sacrificial layer does not decay or influence the TFTs performance.[34, 35] The analysis of the device performance is carried out with the free-standing PDMS layer, already detached from the carrier wafer. In this state, the device layers are buckled. By taking a cross section of the TFT channel region, it shows that the layers are repeatedly bent

to radii below 20 μm (see Fig. S6). This reveals that the minimum bending radius for the device stack is reached when the PDMS membrane is released from the carrier substrate and it is in flat condition. The reflattening of these wrinkles allows the functionality of the devices while mechanical strain (bending and stretching) is applied on the elastomeric substrate. To determine the influence of bending, a TFT and two logic circuits, an inverter and a NAND gate, are used. They are based on one, two or three bottom-gate inverted staggered IGZO TFTs (see *Device Fabrication* section). IGZO [39] is chosen for its high electrical performance (carrier mobility > 10 cm^2/Vs), low deposition temperature and large area deposition capability, representing a good alternative to organic semiconductors.[40] To test the electrical functionality in a macroscopic condition of strain, the devices are characterized while on the wrinkled elastomeric substrate and while bent down to a radius of 2.5 mm. For this experiment, the PDMS membrane is wrapped around a metallic rod using a double side tape (3M 300 LSE, Young's modulus and thickness, E_{tape} = 10 MPa and t_{tape} = 120 μm, respectively). The functionality of the devices, when mechanical strain is applied, is preserved by the reflattening of the wrinkles. Indeed, by bending the devices parallel to the source-drain current direction, the wrinkles disappear along that direction (see Fig. 2a and Fig. S7). The wrinkle profile is simulated after the release and when the PDMS membrane is bent (Fig. 2c). As expected, the amplitude is reduced by 38% while the wavelength is increased by 3%, and the 2D map of the strain tensor ε along the wrinkle profile is presented (see Fig. S8).

The single wrinkled TFTs (W/L = 50 μm /25 μm) are electrically characterized and show similar parameters presented elsewhere (see Fig. S7). [34] The scalability of our process is proved by characterizing the two logic circuits. The inverter (as well as the NAND) is in a pseudo-NMOS configuration and it is composed by a load TFT and a driver TFT (two driver TFTs, for

the NAND). The output characteristic in flat and bent condition, the optical micrographs and are shown in Fig. 2a and 2b.

Stretching. This buckling procedure represents a realistic and customized pathway for stretchable electronics. The physics of the response to the applied strain is similar: the reflattening of the wrinkles allows the accommodation of the strain without damaging the device layers. To prove the feasibility of the buckling approach, the PDMS membrane is mounted on a custom-made stretching setup, using a 2 mm-thick double side adhesive (VHB 4918F, 3M) (see Fig. S9). Similarly to the bending experiments, the mechanical strain is applied parallel to the source-drain current direction. Although the device buckling allows stretchability in both x- and y- direction, the choice for the strain direction is done to avoid capillary cracks and maximize the device functionality while strain is applied.[41] The electrical performance and optical images of a TFT at different stretching stages are presented in Fig. S10 and Fig. S9, respectively. In the strain range from 0% to 5%, the threshold voltage shift ΔV_{th} and the normalized mobility μ/μ_0 have an average variation of 3 mV and 6% (see Fig. S11). Moreover, the on current I_{ON} and off current I_{OFF} show stable trends over the stretching range (I_{ON}/I_{OFF} ratio always greater than 2×10^6). In a similar way, an unipolar IGZO-based wrinkled inverter is AC characterized for different stretching values (Fig. 3a-c). Here, the mechanical strain is applied parallel to the driver TFT (W/L = 280/10 μm). The device stays functional up to 5.1% strain. At this strain value, it exhibits variation with respect to flat condition of 8 μs and 2 μs, for the propagation delays (from low L to high H output voltage levels, $T_{PD\ L->H}$, and from high H to low L, $T_{PD\ H->L}$), and 3 μs and 16 μs, for the fall/rise times (Fig. 3d and 3e). Considering the results in Fig. S3 (for T = 180 °C), similar performance variations are expected while stretching up to 4.5 % is applied perpendicular to the channel direction.

In general, for both bending and stretching tests, the reasons for possible device failure are mainly three: when the release between the carrier wafer and the PDMS is performed, layer delamination may occur (see Fig. S12); cracks in the gate dielectric, which cause high gate leakage current; finally, when the wrinkles are completely reflattened and further strain is applied, irreversible damages (i.e. cracks) in the gate, source and drain metal paths, make impossible to further characterize the devices (see Fig. 3f). Considering this, the main limitation to the flexibility of the devices fabricated with our buckling technique is imposed by the tuning of the wrinkle size (height and amplitude, in Fig. S1), and the wrinkle reflattening, while strain is applied.

Application. Other important requirement for flexible electronics is wireless communication to allow a more versatile technology and unobtrusive data transfer.[42] Moreover, medical implants and health monitoring demand for biocompatibility of the electronics.[6] As a proof of the scalability of our approach, a wrinkled full-wave rectifier is presented in Fig. 4a. It is based on four stretchable NiO/IGZO p-n diodes (see *Device Fabrication* section) in a bridge configuration (see Fig. S13). Differently from previous work [14, 15], the fabrication of this device directly on PDMS allows its implementation in biomedical applications, where bendable and stretchable electronics are required. As an illustrative example, the electrical characterization is carried out when the PDMS membrane is free-standing and when wrapped around the artificial wrist of a mannequin (r = 30 mm) (Fig. 4b). The AC voltage input of 10 V peak-to-peak is transmitted at the input of the rectifier; the output signal, shown in Fig. 4c, is not affected by the mechanical strain.

Together with high flexibility, transparency is an important requirement for applications, such as smart glasses and unobtrusive health monitoring systems.[43] By taking advantage of the high

transparency of the PDMS substrate, IGZO and Al_2O_3 (see Fig. S14), fully transparent and wrinkled TFTs are presented in Fig. 4d, for unobtrusive and flexible electronic applications (see Fig. 4e). In this case, standard metals are replaced by Indium-Tin-Oxide (ITO) (see *Device Fabrication* section) to ensure transparency of the whole device stack up to 71.6% (see Fig. S14). The TFT (W/L = 280 μm/30 μm), characterized after the release of the PDMS membrane from the carrier support, exhibits an effective mobility μ_{eff} of 13.7 cm^2/Vs, threshold voltage V_{th} equal to 0.1 V, I_{ON}/I_{OFF} ratio equal to $1x10^7$ (see Fig. 4f). These findings demonstrate how our buckling approach enables the realization of both transparent and non-transparent TFTs with similar electrical performances.

CONCLUSION

In summary, a systematic approach for the fabrication of flexible and biocompatible electronic devices on PDMS substrate is presented. By tuning the curing temperature of the elastomeric membrane and the oxidation time, the formation of a network of out-of-plane wrinkles with variable amplitude and wavelength is achieved. The strain in the gate dielectric is low enough to allow functionality of the electronic device, even after the buckling phenomenon. In this way, the reflattening of such wrinkles allows TFTs and logic gates (inverter and NAND), directly fabricated on the elastomeric support, to accommodate the strain while bent down to 13 μm bending radii, as well as stretched up to 5%. Moreover, a full-wave rectifier, based on four IGZO/NiO p-n diodes for power transmission system, is electrically characterized on free-standing substrate and wrapped around an artificial human wrist, showing no degradation. As proof of concept, transparent and wrinkled TFTs are also realized, showing comparable performances to the non-transparent ones, which can result in pioneering applications, such as

smart contact lenses or smart glasses. The biocompatibility of the PDMS substrate together with the buckling process presented here prove the high potential for an established route for health monitoring and medical implants.

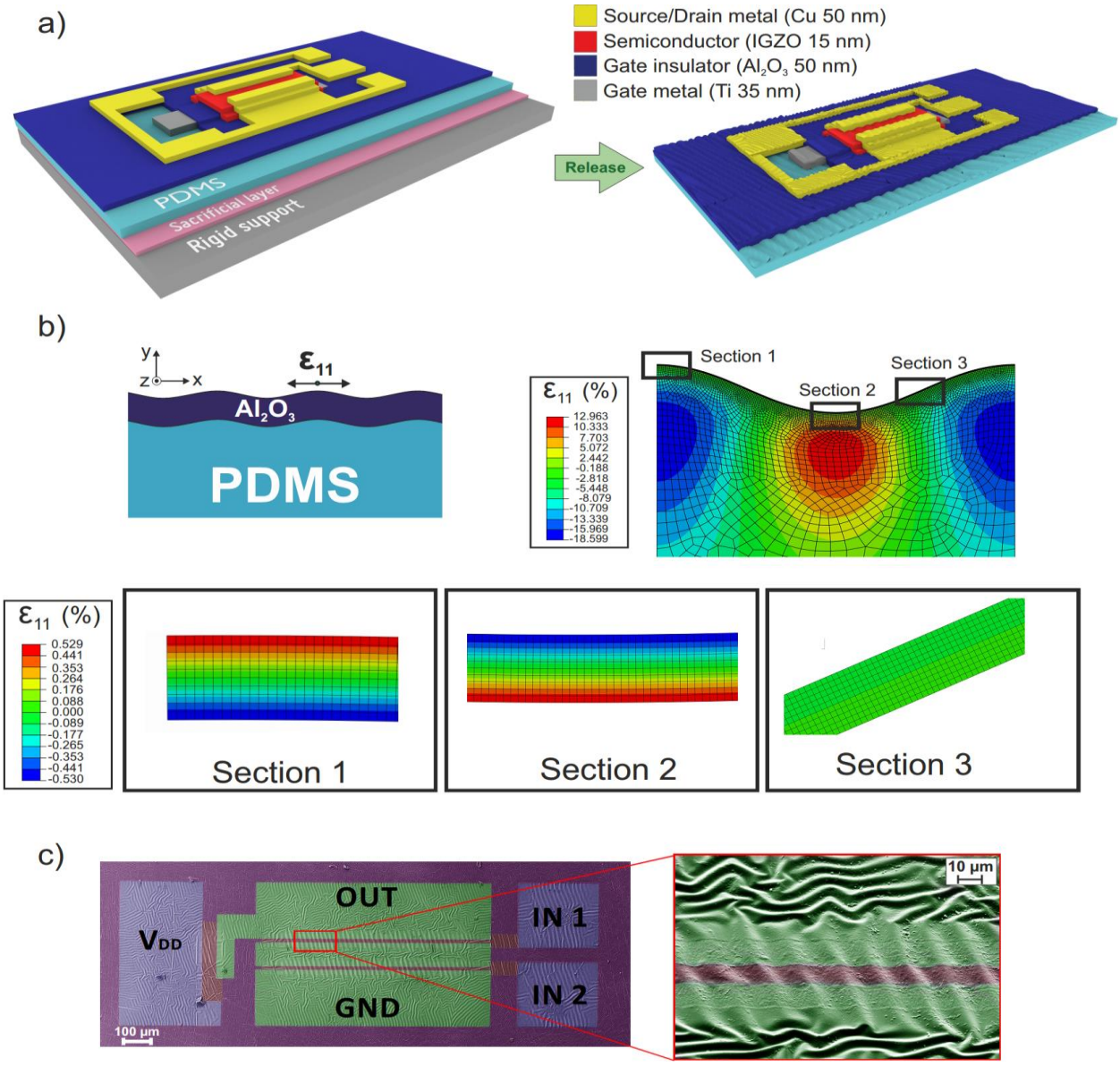
METHODS

Substrate preparation: For the substrate preparation, a Silicon wafer is used as rigid support, coated with a 100 nm thick Polyvinyl Alcohol (PVA) layer (4.7% concentration), acting as sacrificial layer. Then, a 80 µm thick PDMS (Dow Corning Sylgard 184, mixed in a 10:1 weight ratio) is spin coated and cured. Curing temperatures and times are: 180°C for 9 minutes, 150 °C for 10 minutes, 100 °C for 45 minutes, 21 °C for 48 hours.

Device fabrication: The fabrication of IGZO TFTs is described in [34]. For lift-off structuring, the sample is placed in Acetone bath for 14 minutes and then in Isopropyl alcohol (IPA) for 4 minutes. Low ultrasonic power is required. To get access to the gate pads, contact vias are structured and etched by a 50 ml H_2O + 45 ml CH_3COOH (acetic acid) + 10 ml HNO_3 (nitric acid) + 250 ml H_3PO_4 (phosphoric acid) solution, heated to a temperature of 50 °C for 30 seconds. For source and drain contacts, a wet etching process in Iron chloride solution (156 mg Iron chloride ($FeCl_3$) + 364 ml H_2O) for 10 seconds is performed. For the transparent TFTs, 100 nm-thick ITO layer is deposited by RF sputtering at room temperature for the gate, source and drain contacts, and then structured by lift-off. The rectifier consists of 35 nm Ti layer, acting as anode metal, and structured by lift-off. Then, as p- and n-type semiconductor, 100 nm NiO and IGZO are, respectively, DC and RF sputtered at room temperature. The former is structured by lift-off process, while the latter one, by wet etching. Finally, 50 nm Cu are evaporated at

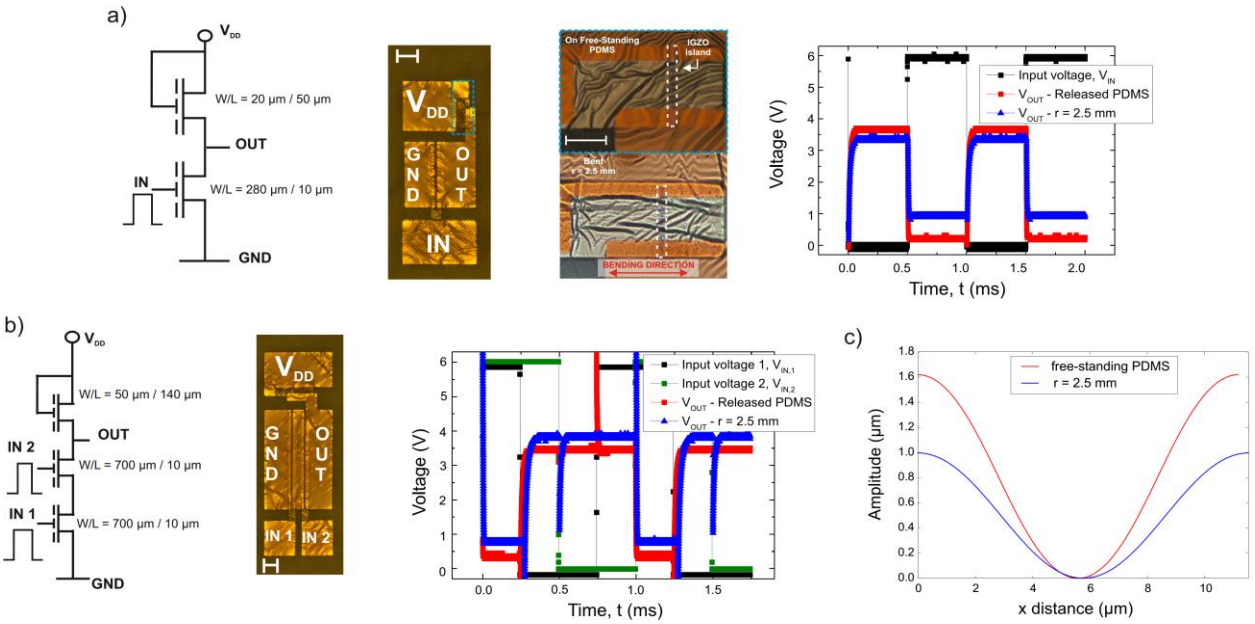
deposition rate of ~ 1 nm/s, acting as top metal contact, and structured by wet etching. For the layer structuring, for TFTs, circuits and rectifiers, standard UV lithography is used.

Electrical Characterization: Devices are characterized by using an Agilent B1500A parameter analyzer under ambient conditions. The bending experiments are described in [34], while for the stretching ones, a custom-made setup is implemented (see Fig. S9). Furthermore, for the AC circuit characterization, a HP 6626A power supply, an Agilent MSO-X-3014A oscilloscope and an Agilent 33522A waveform generator are used.

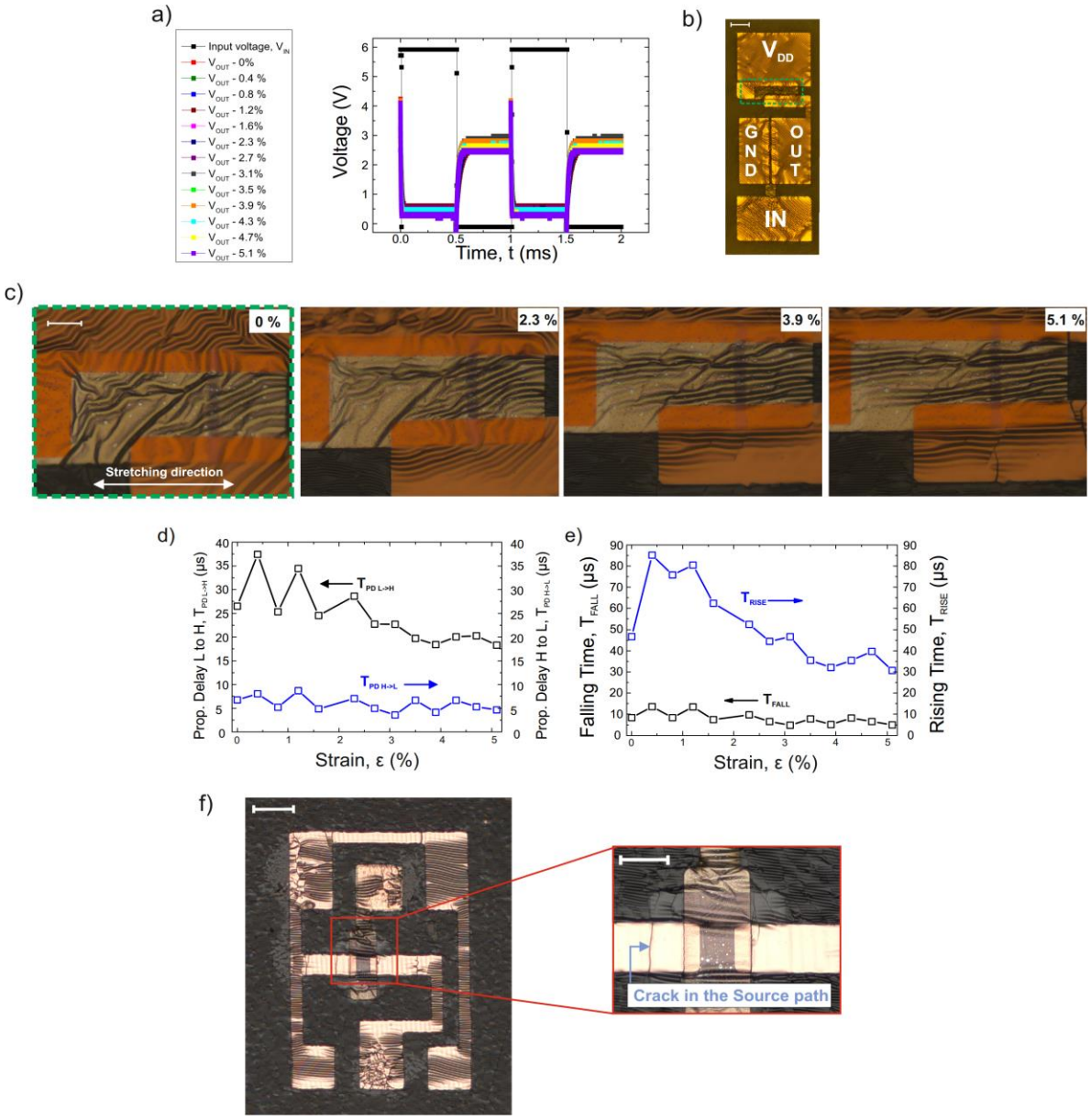


"Figure 1. Wrinkle formation. a) Schematic representation of the device stack (materials and layer thickness) for a wrinkled TFT before and after the release from a carrier support. The devices are fabricated using an inverted staggered bottom gate configuration, using amorphous-IGZO as semiconductor layer and a maximum fabrication temperature of 150 °C. b) 2D colored strain map of the ε_{11} strain component. In this case, the simulation refers to a PDMS layer cured at 180°C with an O_2 plasma treatment of 1 min, with a 50 nm-thick Al_2O_3 layer deposited on top.

In the color bar, positive strain (in red) corresponds to tensile strain, while, negative strain (in blue) corresponds to compressive strain. Moreover, the color maps of three sections are highlighted to show the alternation of positive strain, 0%-strain and negative strain areas along a single wrinkle profile. c) Colored SEM image of a wrinkled unipolar logic NAND gate and its channel region."

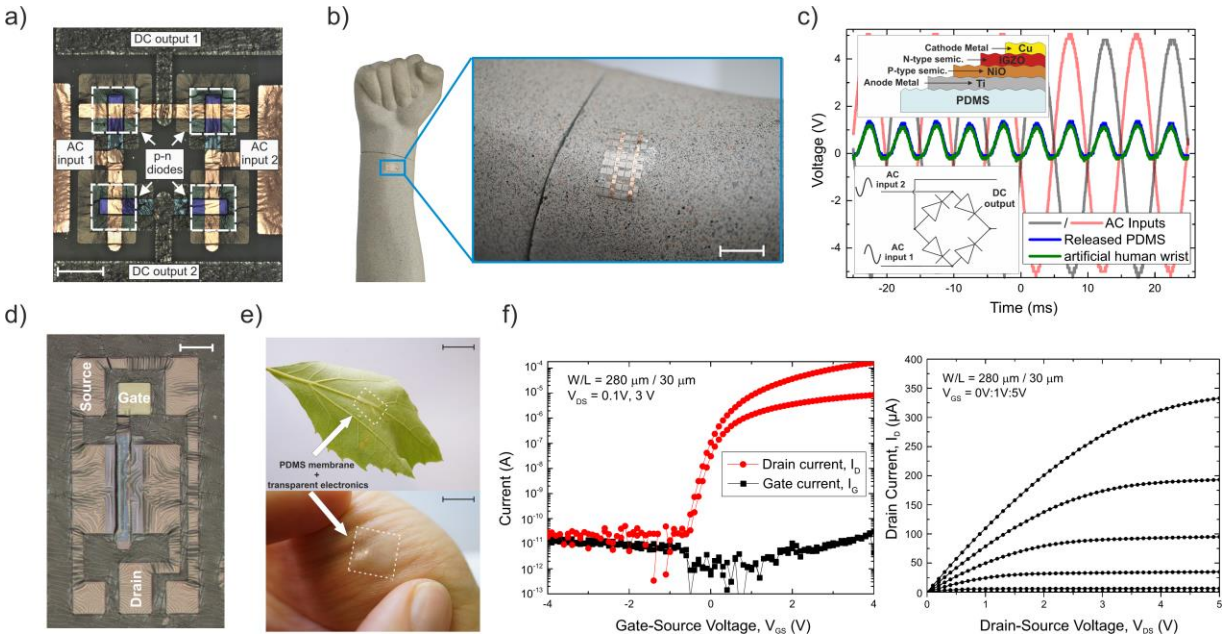


"Figure 2. Circuit performances under bending experiments. Although the device layers are submitted to curvature radii below 20 µm after thermal stress releasing in the flexible substrate, the circuit performances are evaluated while a macroscopic bending strain is applied on the PDMS membrane. Schematic, optical image and output of (a) an unipolar inverter (supply voltage V_{DD} = 10 V and input voltage V_{IN} = 0 V − 6 V) (Scale bar: 100 µm) and (b) an unipolar logic NAND gate (supply voltage V_{DD} = 10 V and input voltages V_{IN-1} = V_{IN-2} = 0 V − 6 V) (Scale bar: 100 µm). For the inverter in (a), an optical image of the load TFT on a free standing PDMS membrane and bent to a radius of 2.5 mm is shown (Scale bar: 100 µm). Due to the bending strain, the stress is accommodated by reflattening the wrinkles. For both circuits, the bending direction is parallel to the source-drain current direction of the driver TFTs. (c) Simulated profiles of a wrinkle in a released PDMS membrane and when bent to r = 2.5 mm."



"Figure 3. Circuit performances under stretching condition and device failure. Output (a) and optical image (b) (Scale bar: 100 µm) of an unipolar IGZO-based inverter up to 5.1 %. (c) The evolution of the wrinkles in the green box in (b) at different stretching values is shown (Scale bar: 25 µm). Here, the stretching direction is applied parallel to the source-drain current direction of the driver TFT and input voltage V_{IN} = 0 V − 6 V. d) Propagation delays (from low to high $T_{PD\ L->H}$, black square, and from high to low $T_{PD\ H->L}$, blue square) and (e) falling/rising times

(T_{FALL}, black square, T_{RISE}, blue square) for an unipolar inverter with driver and load TFTs of 280 μm/ 10 μm and 20 μm/ 50 μm, respectively. (f) When high strain is applied ($\varepsilon > 5$ %), possible cracks in the metal paths permanently harm the electrical characterization of the device. Here, a TFT is intentionally stretched at strain values above 5 % (Scale bar: 100 μm), with crack formation near its channel region (Scale bar: 50 μm). ”



"Figure 4. Wrinkled rectifier and transparent TFT for stretchable applications. a) Micrograph of a full-wave rectifier based on IGZO/NiO semiconductors in a bridge configuration (scale bar = 300 µm). b) Demonstration of wrinkled circuit in real life. Using an additional 120 µm-thick double side tape (3M 300LSE), a PDMS membrane is wrapped around mannequin wrist (r = 30 mm) (Scale bar: 1 cm). (c) The input signals have peak-to-peak input voltages of 10 V, provided at a frequency of 100 Hz. The transmitted voltage is not affected by the strain due to the non-flat surface of the artificial wrist. In the insets, a cross section of the diode and a circuit schematic are presented. d) Micrograph of a transparent TFT (Scale bar: 100 µm) and e) transfer of the PDMS membrane with the transparent electronics on plant leaf and on human skin (Scale bar: 1 cm). f) Transfer and output characteristics of a wrinkled and transparent TFT. Characterized after the release of the PDMS membrane from the carrier support, it shows an effective mobility μ_{eff}, threshold voltage V_{th}, subthreshold swing SS and I_{ON}/I_{OFF} ratio equal to 13.7 cm^2/Vs, 0.1 V, 0.13 V/dec and $1x10^7$."

ASSOCIATED CONTENT

Supporting Information.

The tuning of the wrinkle size on the surface PDMS membrane, the PDMS release process from the carrier wafer, a comparison of surface area reduction among samples with different PDMS curing temperature, a wrinkle profile and strain analysis, a wrinkle profile in the channel region of a logic NAND gate, the minimum bending radius in the channel region, the TFT performance during bending, the simulated 2D model and cross-sectional strain map in the Al_2O_3 layer, the wrinkled TFT stretching, the TFT performances under stretching condition, the TFT parameter variations during stretching, the reasons for device failure, a buckled diode and a transparent TFT are presented.

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Author Contributions

G.C. conceived the work and wrote the manuscript. G.C, C.V., N.M., P.A., L.P., A.D., S.K., L.B., G.A.S. carried out the experiments and characterization. R.H. simulated the mechanics of the system. G.T. supervised the work.

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Notes

The authors declare no competing financial interest.

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